Claims

[c1] 1. A storage capacitor structure, comprising:a first capacitor electrode on a substrate;a capacitor dielectric layer on the first capacitor electrode; a second capacitor electrode on the capacitor dielectric layer, wherein the second capacitor electrode has a surface area smaller than the first capacitor electrode; a passivation layer on the second capacitor electrode, wherein the passivation layer has an opening that exposes a portion of the second capacitor electrode; and a pixel electrode layer on the passivation layer such that the pixel electrode layer and the second capacitor electrode are electrically connected through the opening in the passivation layer.

[c2] 2. The capacitor structure of claim 1, wherein an overlapping region between the first capacitor electrode and the second capacitor electrode is substantially equal to the area of the second capacitor electrode.

[c3] 3. The capacitor structure of claim 1, wherein the pixel electrode is further connected to a switching element.

[c4] 4. The capacitor structure of claim 1, wherein the pixel electrode is further connected to a thin film transistor.

[c5] 5. The capacitor structure of claim 1, wherein the first capacitor electrode is further connected to a common voltage.

[c6] 6. A storage capacitor structure, comprising:a first capacitor electrode on a substrate;a capacitor dielectric layer on the substrate; and a second capacitor electrode on the capacitor dielectric layer, wherein the edges of the second capacitor electrode are bounded within the edges of the first capacitor electrode.

[c7] 7. The capacitor structure of claim 6, wherein the structure further includes: a passivation layer over the second capacitor electrode, wherein the passivation layer has an opening that exposes a portion of the second capacitor electrode; and a pixel electrode layer on the passivation layer such that the pixel electrode layer and the second capacitor electrode are electrically connected through the opening in the passivation layer.

[c8] 8. The capacitor structure of claim 6, wherein residual conductive residual material is distributed along the edges of the first capacitor electrode.

[c9] 9. The capacitor structure of claim 8, wherein the residual conductive residual material includes amorphous silicon.

[c10] 10. The capacitor structure of claim 6, wherein a thin film transistor controls the storage capacitor comprising of the first capacitor electrode and the second capacitor electrode.

[c11] 11. A method for forming a storage capacitor, comprising the steps of:forming a first capacitor electrode on a substrate;forming a capacitor dielectric layer on the first capacitor electrode; forming a second capacitor electrode on the capacitor dielectric layer, wherein the second capacitor electrode has a surface area smaller than the first capacitor electrode; forming a passivation layer on the second capacitor electrode; patterning the passivation layer to form an opening that exposes a portion of the second capacitor electrode; and forming a pixel electrode layer on the passivation layer such that the pixel electrode layer and the second capacitor electrode are electrically connected through the opening in the passivation layer.

[c12] 12. The method of claim 11, wherein the overlapping region between the first capacitor electrode and the second capacitor electrode has an area substantially equal to the area of the second capacitor electrode.

[c13] 13. The method of claim 11, wherein the pixel electrode is further connected to a switching element.

[c14] 14. The method of claim 11, wherein the pixel electrode is further connected to a thin film transistor.

[c15] 15. The method of claim 11, wherein the first capacitor electrode is further connected to a common voltage.

[c16] 16. A liquid crystal display device, comprising:a plurality of scan lines;a plurality of signal lines; and a plurality of pixels each including a liquid crystal cell having a pixel electrode connected to a storage capacitor and a switching element

connected between the liquid crystal cell and one of the signal lines, a gate of the switching element being connected to one of the scan lines; wherein a first capacitor electrode, a capacitor dielectric layer and a second capacitor electrode together form the storage capacitor, and an overlapping region between the second capacitor electrode and the first capacitor electrode has an area substantially equal to the area of the second capacitor electrode.

Add A3